EUTECH MICROELECTRONICS

2.5-W/CH Stereo Filter-less Class-D Audio Power Amplifier with Auto-Recovery

DESCRIPTION

The EUA2012A is a high efficiency, 2.5W/channel stereo class-D audio power amplifier. A low noise, filterless PWM architecture eliminates the output filter, requiring only two external components for operation.

Operating from a single 5V supply, EUA2012A is capable of delivering 2.5W/ channel of continuous output power to a 4Ω load with 10% THD+N.

The EUA2012A features independent shutdown controls for each channel. The gain can be selected to 6, 12, 18, or 24 dB utilizing the G0 and G1 gain select pins. High PSRR and differential architecture provide increased immunity to noise and RF rectification.

The EUA2012A is available in space-saving WCSP, TQFN and TSSOP packages, is an idea choice for mobile phones and other portable communication devices.

FEATURES

- Low EMI Emission
- Output Power By TQFN Package
  - 2.5W/Ch Into 4Ω at 5V
  - 1.6W/Ch Into 8Ω at 5V
  - 800mW/Ch Into 8Ω at 3.6V
- Wide Supply Voltage: 2.5V to 5.5V
- Independent Shutdown Control for Each Channel
- Selectable Gain of 6,12,18 and 24 dB
- High PSRR :63dB at 217Hz
- Fast 34ms Startup Time
- Low 5mA Quiescent Current at 3.6V Supply and 1.5μA Shutdown Current
- Short-Circuit Auto-Recovery and Thermal Protection
- Space Saving Packages
  - 4mm×4mm TQFN-20 package
  - 2mm×2mm WCSP-16 package
  - TSSOP-20 package
- RoHS Compliant and 100% Lead(Pb)-Free, Halogen-Free

APPLICATIONS

- Wireless or Cellular Handsets and PDAs
- Portable Audios
- Notebook PC

Typical Application Circuit

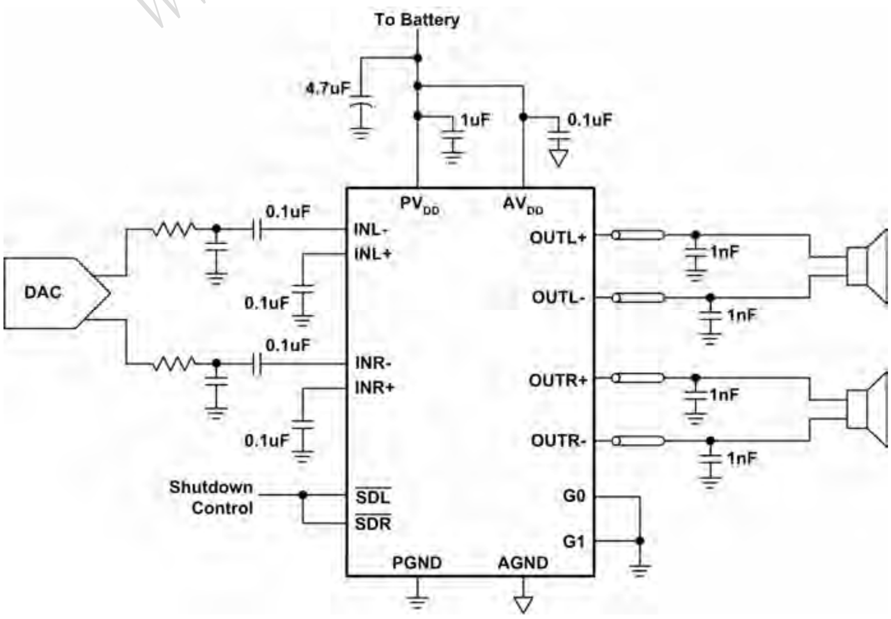
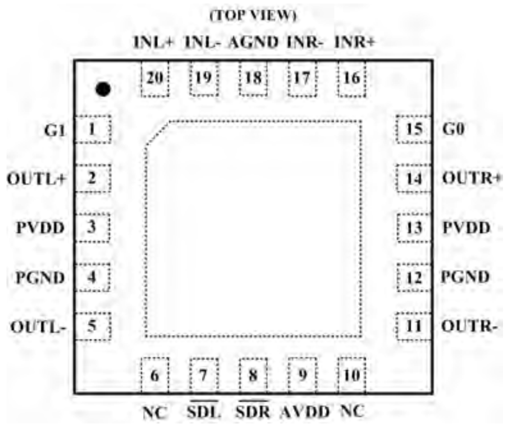
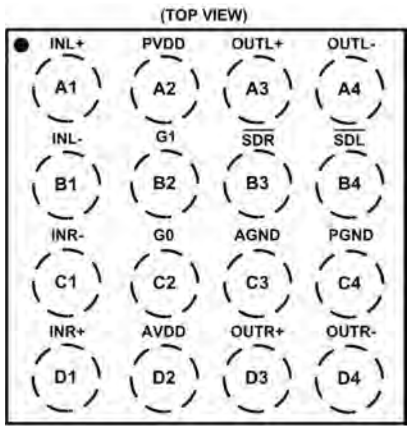
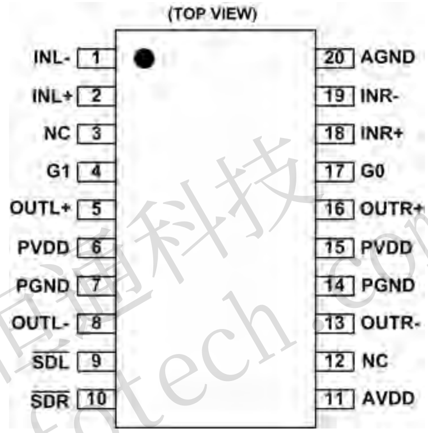


Figure1.

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
TQFN-20		WCSP-16	
TSSOP-20			

Pin Description

PIN	TQFN-20	WCSP-16	TSSOP-20	I/O	DESCRIPTION
INR+	16	D1	18	I	Right channel positive input
INR-	17	C1	19	I	Right channel negative input
INL+	20	A1	2	I	Left channel positive input
INL-	19	B1	1	I	Left channel negative input
$\overline{SDR}$	8	B3	10	I	Right channel shutdown terminal (active low)
$\overline{SDL}$	7	B4	9	I	Left channel shutdown terminal (active low)
G0	15	C2	17	I	Gain select (LSB)
G1	1	B2	4	I	Gain select (MSB)
PVDD	3,13	A2	6,15	I	Power supply (Must be same voltage as AVDD)
AVDD	9	D2	11	I	Analog supply (Must be same voltage as PVDD)
PGND	4,12	C4	7,14	I	Power ground
AGND	18	C3	20	I	Analog ground
OUTR+	14	D3	16	O	Right channel positive differential output
OUTR-	11	D4	13	O	Right channel negative differential output
OUTL+	2	A3	5	O	Left channel positive differential output
OUTL-	5	A4	8	O	Left channel negative differential output
NC	6,10	-	3,12	-	No internal connection

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2012AHIR1	WCSP-16	xxx H0	-40 °C to +85°C
EUA2012AJIR1	TQFN-20	xxxxx 2012A	-40 °C to +85°C
EUA2012AQIR1	TSSOP-20	xxxxx EUA2012A	-40 °C to +85°C

EUA2012A □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen-Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  J: TQFN
  H: WCSP
  Q: TSSOP

Block Diagram

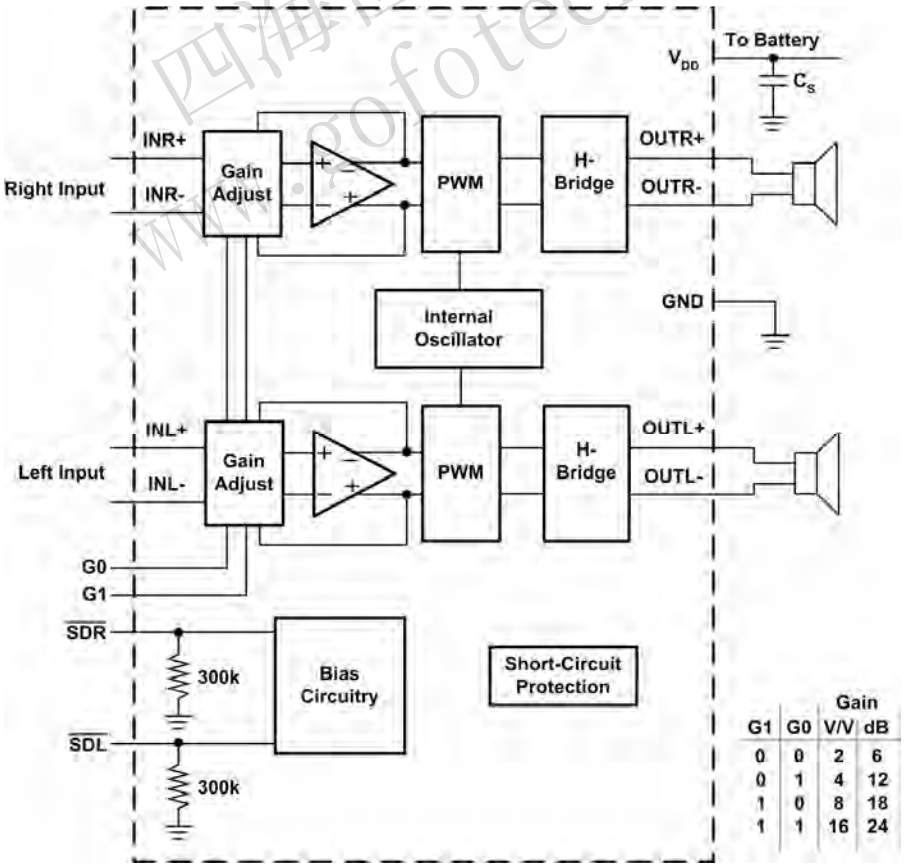


Figure 2.

Absolute Maximum Ratings (1)

- Supply Voltage, AVDD,PVDD -- -0.3 V to 6V
- Input Voltage, V_I -- -0.3 V to V_{DD} +0.3V
- Junction Temperature, T_J --- -40°C to 150°C
- Storage Temperature Rang, T_{stg} -- -65°C to 85°C
- ESD Susceptibility -- 2kV
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds -------------------------------------- 260°C
- Thermal Resistance
  - θ_{JA} (TQFN-20) -- 45°C/W
  - θ_{JA} (WCSP-16) -- 105°C/W
  - θ_{JA} (TSSOP-20) --- 92°C/W

Recommended Operating Conditions (2)

	Min	Max	Unit
Supply voltage, AVDD,PVDD	2.5	5.5	V
High-level input voltage, $\overline{SDL}$, $\overline{SDR}$,G0,G1	1.3		V
Low-level input voltage, $\overline{SDL}$, $\overline{SDR}$,G0,G1		0.35	V
Operating free-air temperature, T_A	-40	85	°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics T_A = +25°C (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2012A			Unit
			Min	Typ	Max.	
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	Inputs ac grounded, $A_{V=}$ 6dB, V_{DD}=2.5V to 5.5V		5	25	mV
PSRR	Power supply rejection ratio	V_{DD}= 2.5V to 5.5V		-75	-55	dB
V_{icm}	Common-mode input voltage		0.5		VDD-0.8	V
CMRR	Common-mode rejection ration	Input shorted together, V_{DD}= 2.5V to 5.5V		-69	-50	dB
$\lvert I_{IH} \rvert$	High-level input current	V_{DD}= 5V, V_I= V_{DD}			50	μA
$\lvert I_{IL} \rvert$	Low-level input current	V_{DD}= 5V, V_I= 0V			5	μA
I_{DD}	Supply current	V_{DD}= 5V, no load or output filter		6.2	12	mA
		V_{DD}= 3.6V, no load or output filter		5.2	7.5	
		V_{DD}= 2.5V, no load or output filter		4.5	6	
		Shutdown mode			1.5	μA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{DD}= 5V		400		mΩ
		V_{DD}= 3.6V		450		
		V_{DD}= 2.5V		550		
	Output impedance in $\overline{SHUTDOWN}$ mode	$V_{(\overline{SDR},\overline{SDL})}$=0.35V		2		kΩ
$f_{(sw)}$	Switching frequency	V_{DD}= 2.5V to 5.5V	250	300	350	kHz

Electrical Characteristics T_A = +25°C, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2012A Min	EUA2012A Typ	EUA2012A Max.	Unit
	Closed-loop voltage gain	G0,G1=0.35V		5.3	6	6.5	dB
		G0=V_{DD} ,G1=0.35V		11.2	12	12.5	
		G0=0.35V,G1= V_{DD}		17.2	18	18.5	
		G0,G1= V_{DD}		23	24	24.5	
P_O	Output power (per channel)	RL=8Ω	V_{DD}= 5V,f=1kHz,THD=10%		1.6		W
			V_{DD}= 3.6V,f=1kHz,THD=10%		0.8		
		RL=4Ω	V_{DD}= 5V, ,f=1kHz,THD=10%		2.5		
THD+N	Total harmonic distortion plus noise	P_O=1W,V_{DD}= 5V,A_V=6dB,f=1kHz			0.13		%
		P_O=0.5W,V_{DD}= 5V,A_V=6dB,f=1kHz			0.11		
	Channel crosstalk	f=1kHz			-82		dB
k_{SVR}	Supply ripple rejection ratio	V_{DD}= 5V,A_V=6dB,f=217 Hz			-62		dB
		V_{DD}= 3.6V,A_V=6dB,f=217 Hz			-63		
CMRR	Common mode rejection ratio	V_{DD}= 3.6V,V_{IC}=1V_{PP},f=217 Hz			-60		dB
	Input impedance	A_V=6dB			30.8		kΩ
		A_V=12dB			18.6		
		A_V=18dB			12.4		
		A_V=24dB			6.3		
	Start-up time from shutdown	V_{DD}= 3.6V			34		ms
	Output voltage noise	V_{DD}= 3.6V,f=20 to 20kHz,Inputs are ac grounded, A_V=6dB	No weighting		56		μV
			A weighting		39		

Typical Operating Characteristics

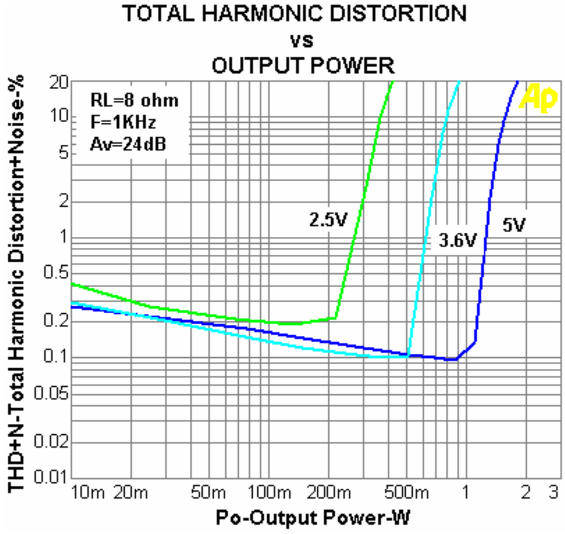


Figure3.

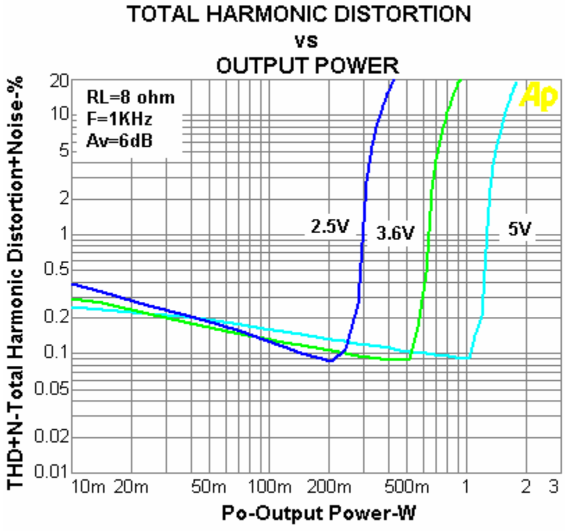


Figure4.

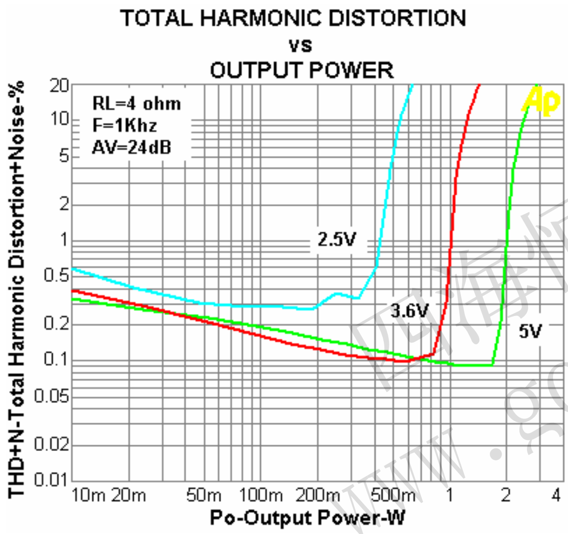


Figure5.

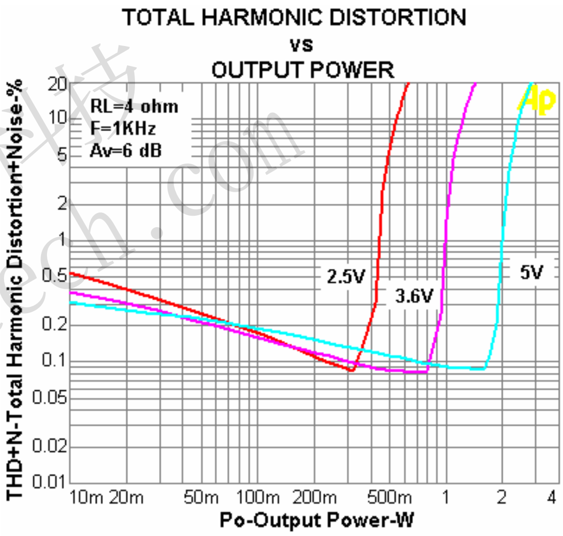


Figure6.

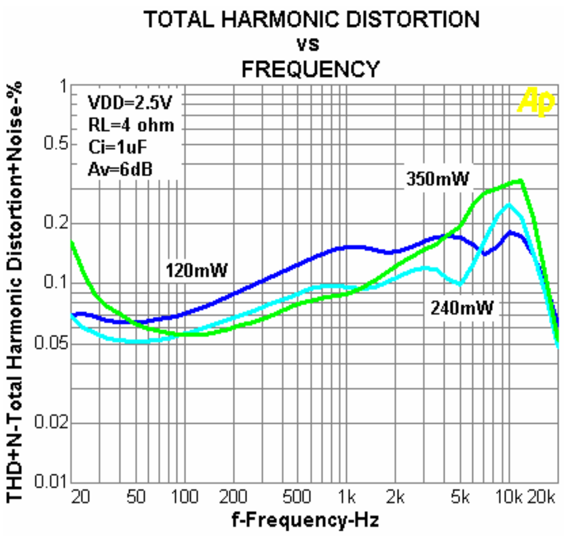


Figure7.

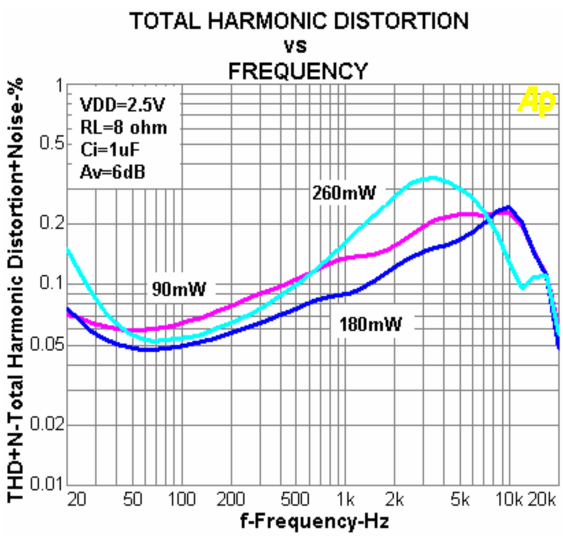


Figure8.

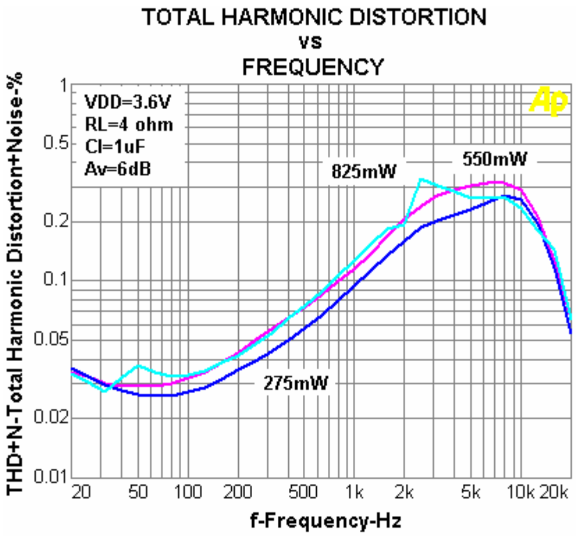


Figure9.

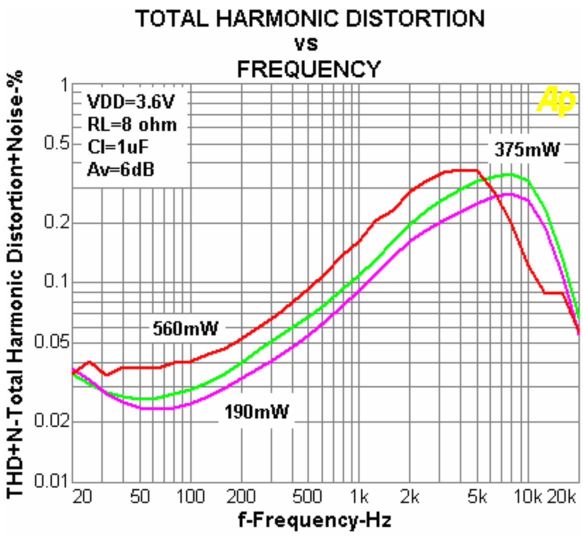


Figure10.

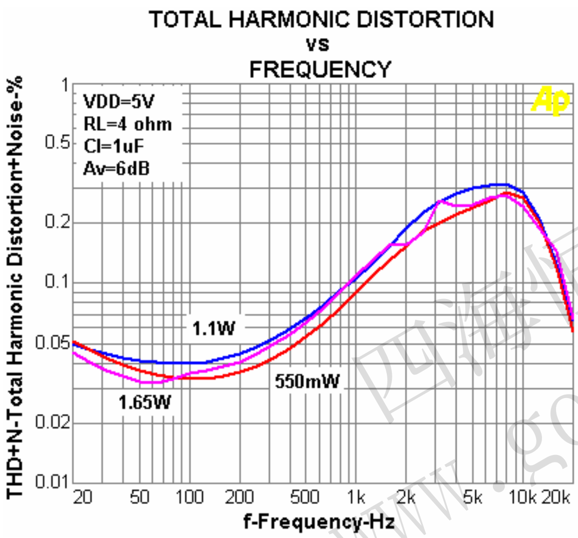


Figure11.

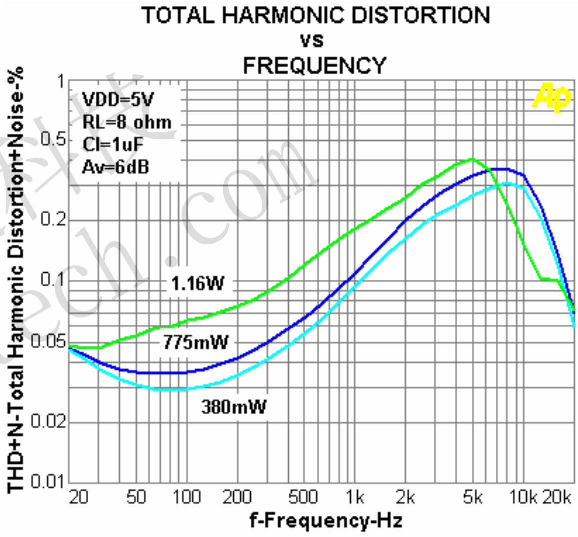


Figure12.

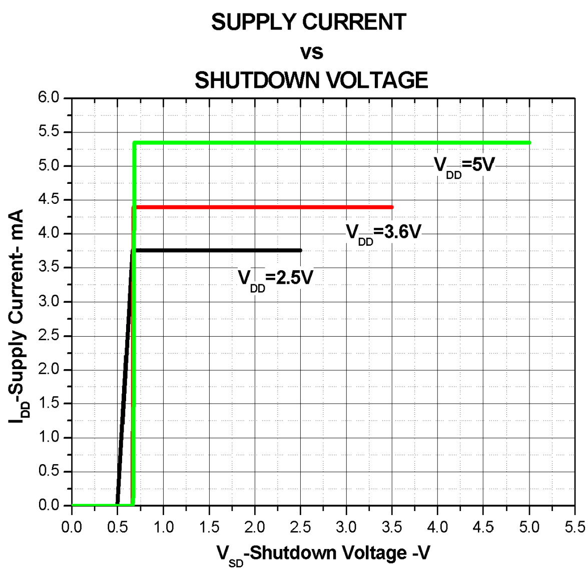


Figure13.

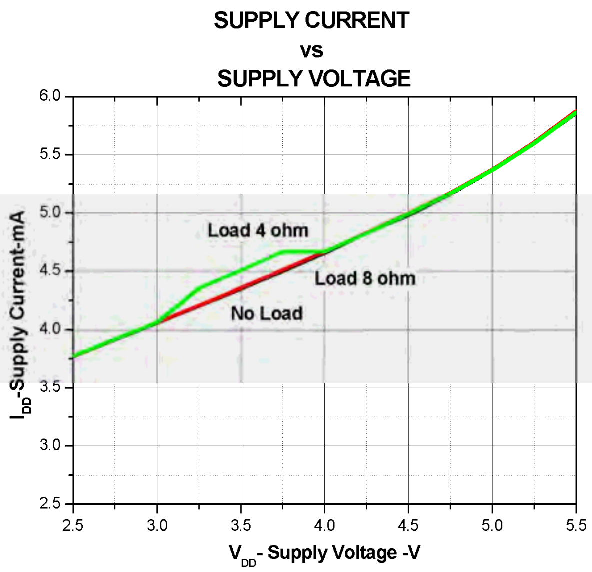


Figure14.

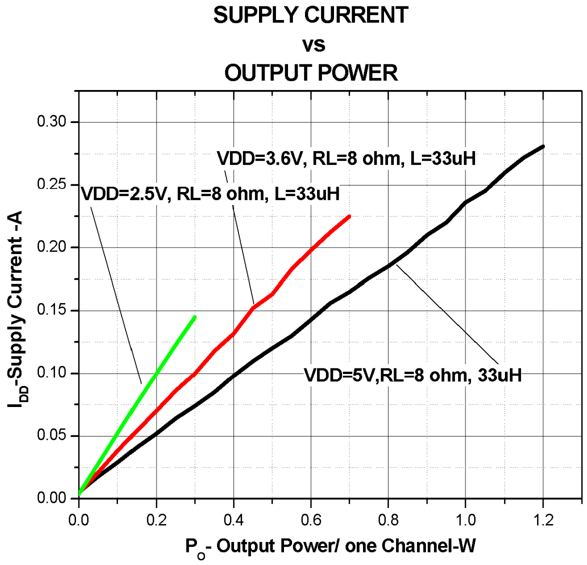


Figure15.

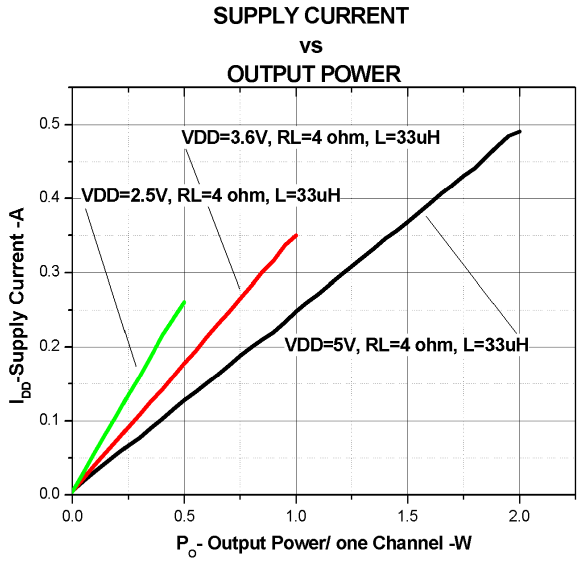


Figure16.

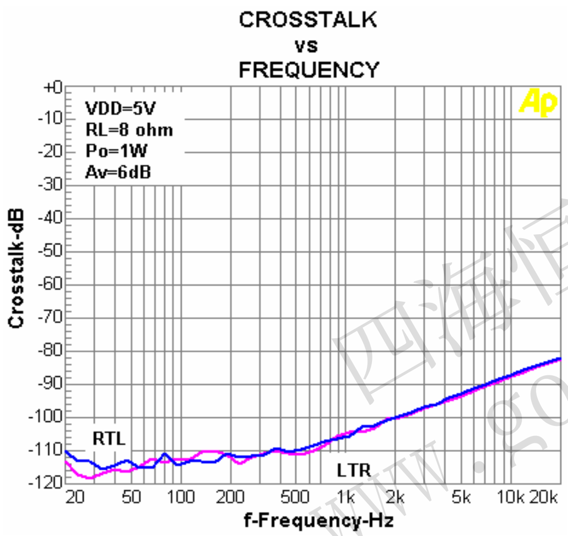


Figure17.

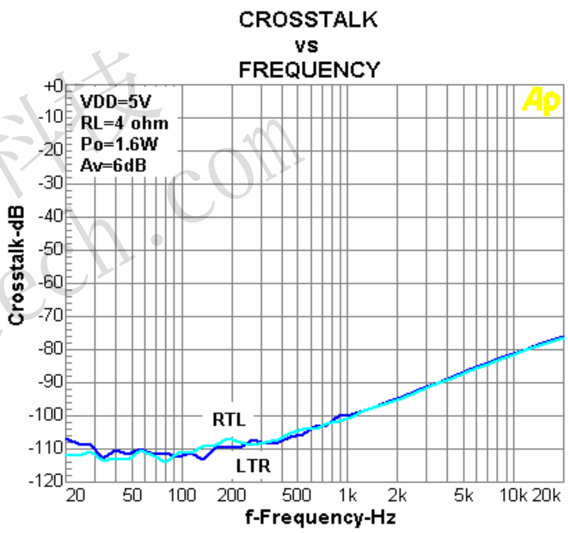


Figure18.

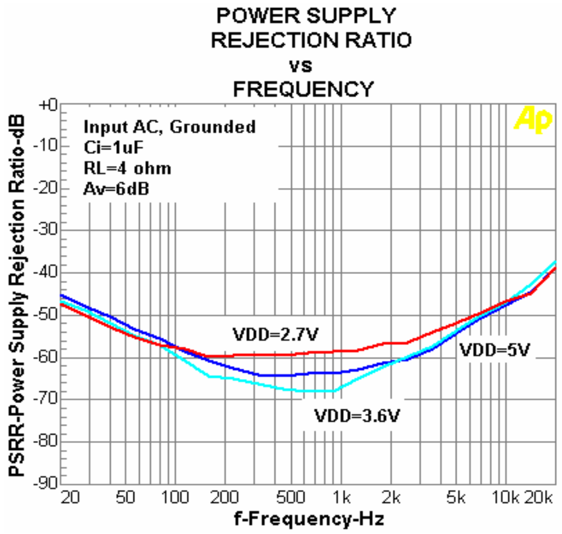


Figure19.

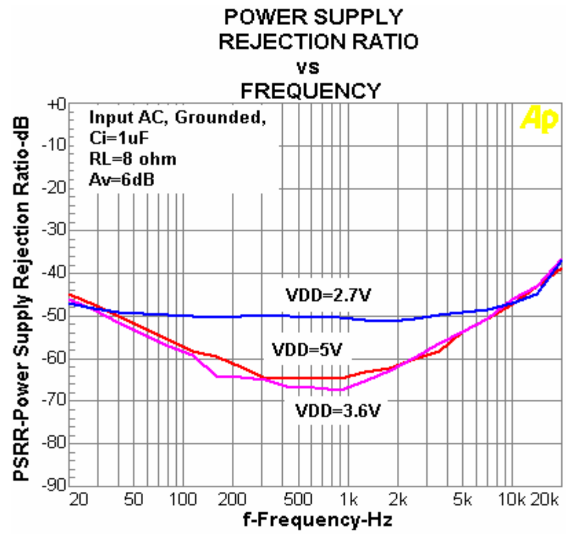


Figure20.

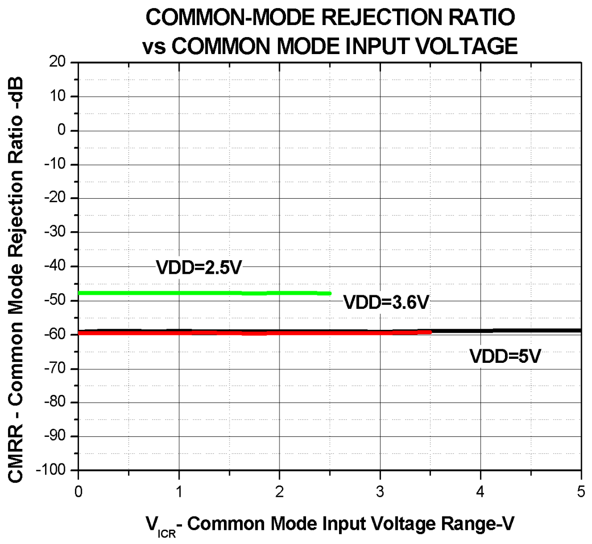


Figure21.

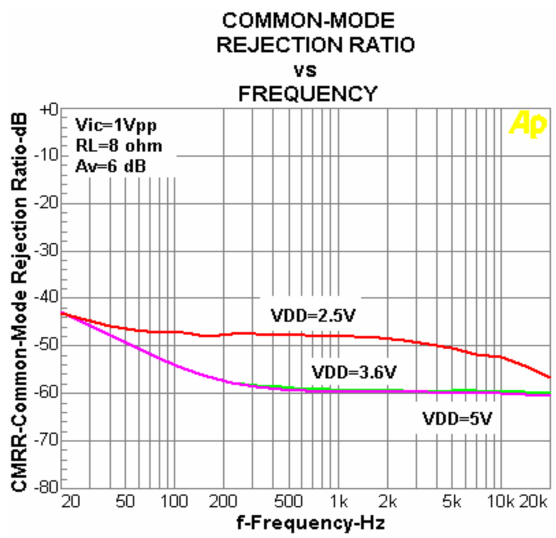


Figure22.

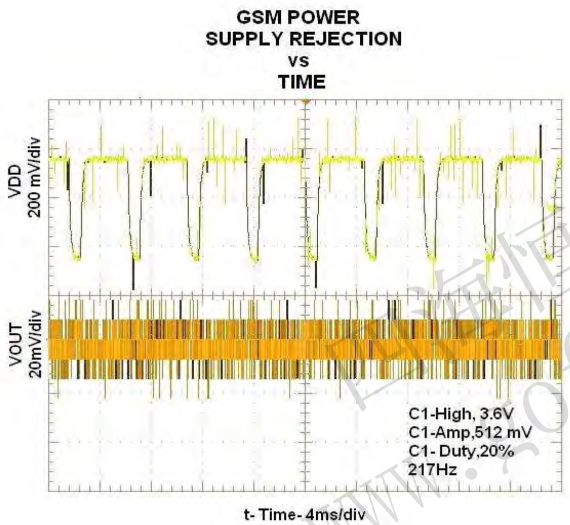


Figure23.

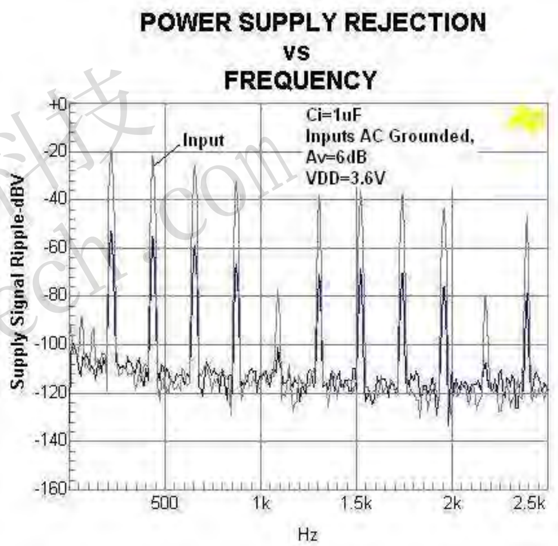


Figure24.

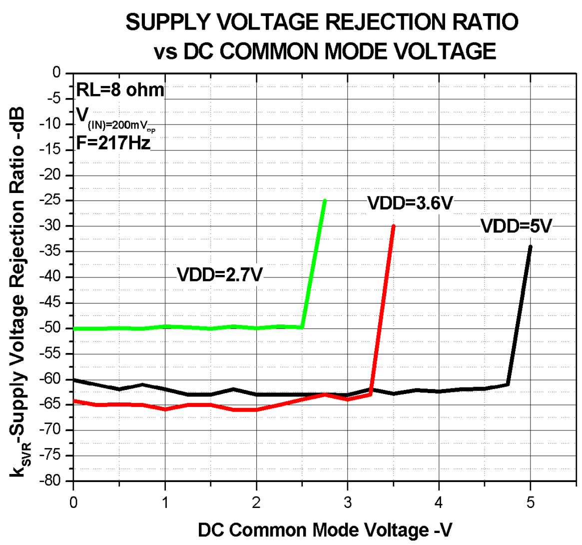


Figure25.

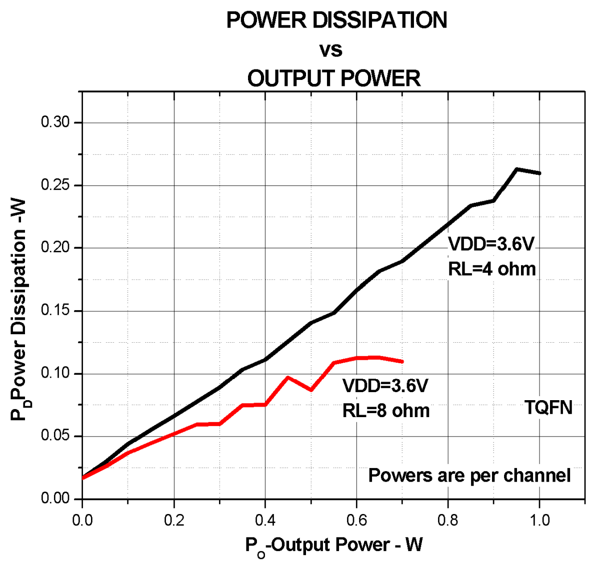


Figure26.

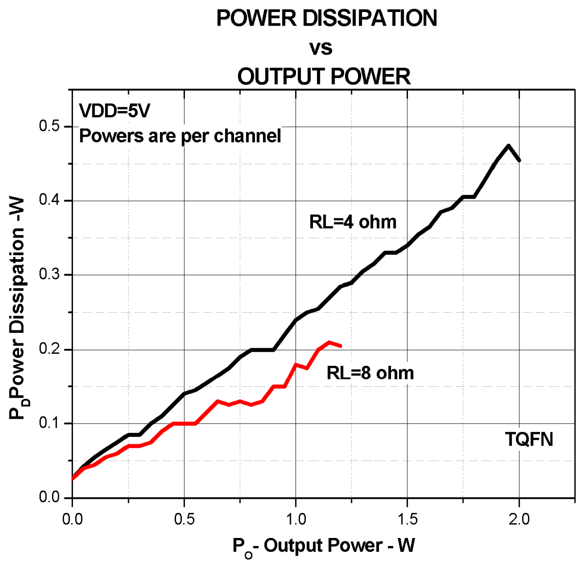


Figure27.

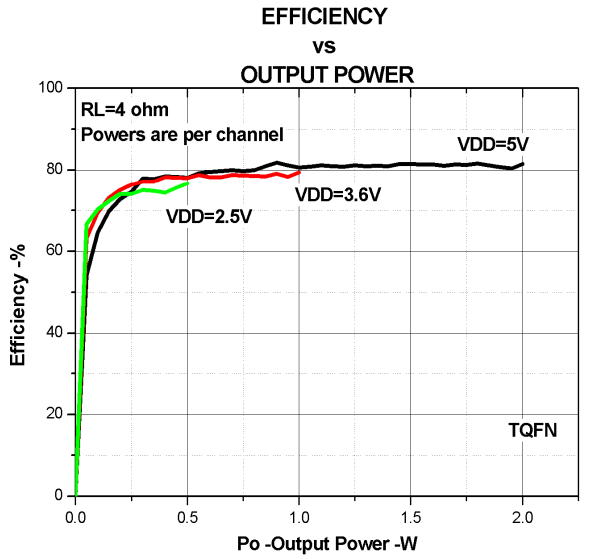


Figure28.

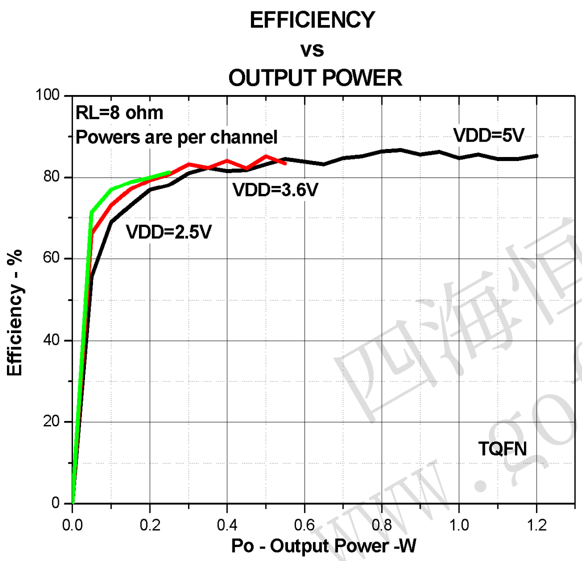


Figure29.

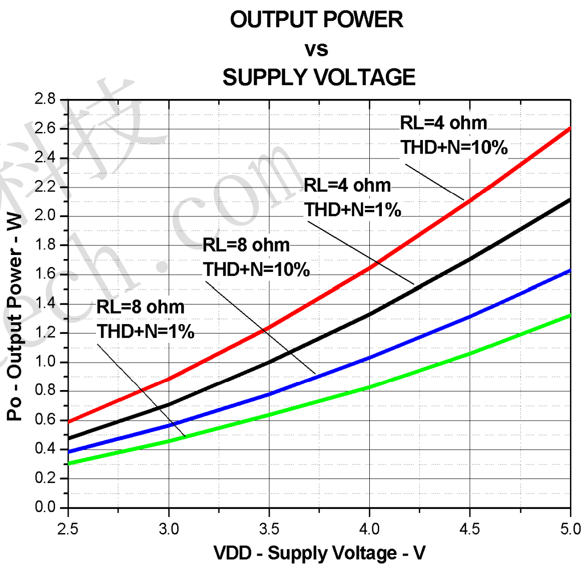


Figure30.

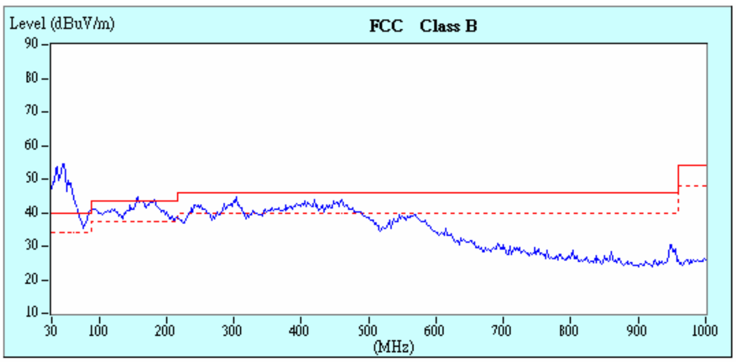


Figure31.

Application Information

Decoupling Capacitor (C_S)

The EUA2012A is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device PV_{DD} lead works best. Placing this decoupling capacitor close to the EUA2012A is important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Table 1. Gain Setting

G1	G0	GAIN (V/V)	GAIN (dB)	Input Impedance (R_I)(KΩ)
0	0	2	6	30.8
0	1	4	12	18.6
1	0	8	18	12.4
1	1	16	24	6.3

Input Capacitors (C_I)

The EUA2012A does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD} – 0.8 V. If the input signal is not biased within the recommended common −mode input range, if high pass filter (shown in Figure 32), or if using a single-ended source (shown in Figure 33), input coupling capacitors are required.
The input capacitors and input resistors form a high-pass filter with the corner frequency, fc, determined in equation (1).

$$f_c = \frac{1}{(2\pi R_I C_I)} \quad \text{--(1)}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset.
Equation (2) is used to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi R_I f_c)} \quad \text{--(2)}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

Component Location

Place all the external components very close to the EUA2012A. Placing the decoupling capacitor, CS, close to the EUA2012A is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Filter Free Operation and Ferrite Bead Filters

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and very low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 34 shows typical ferrite bead and LC output filters.

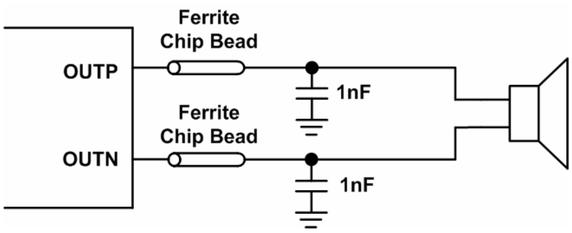


Figure34. Typical Ferrite Chip Bead Filter

Short Circuit Auto-Recovery

When a short circuit event happens, the EUA2012A goes to shutdown mode and tries to reactivate itself after 4ms. This auto-recovery will continue until the short circuit events is removed.

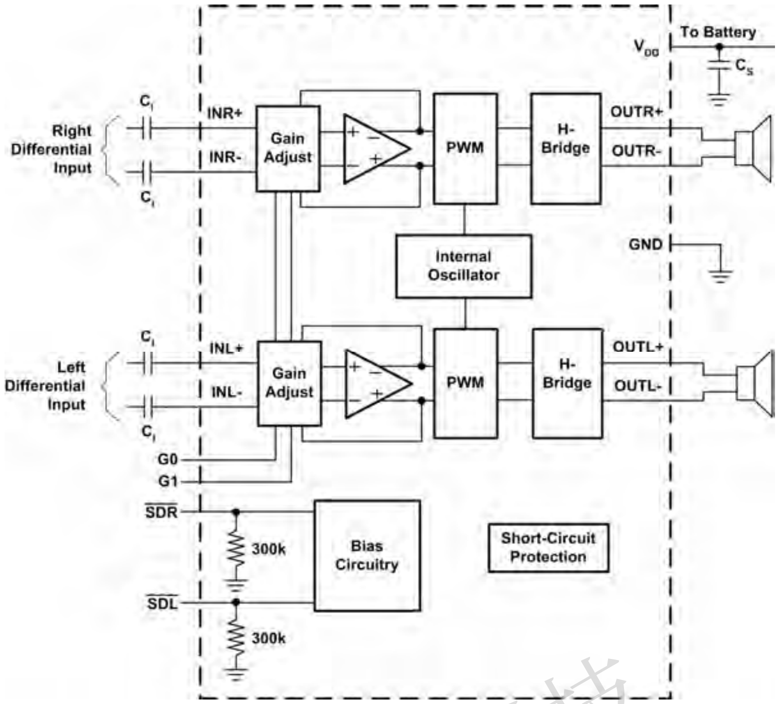


Figure32. Application Schematic With Differential Input and Input Capacitors

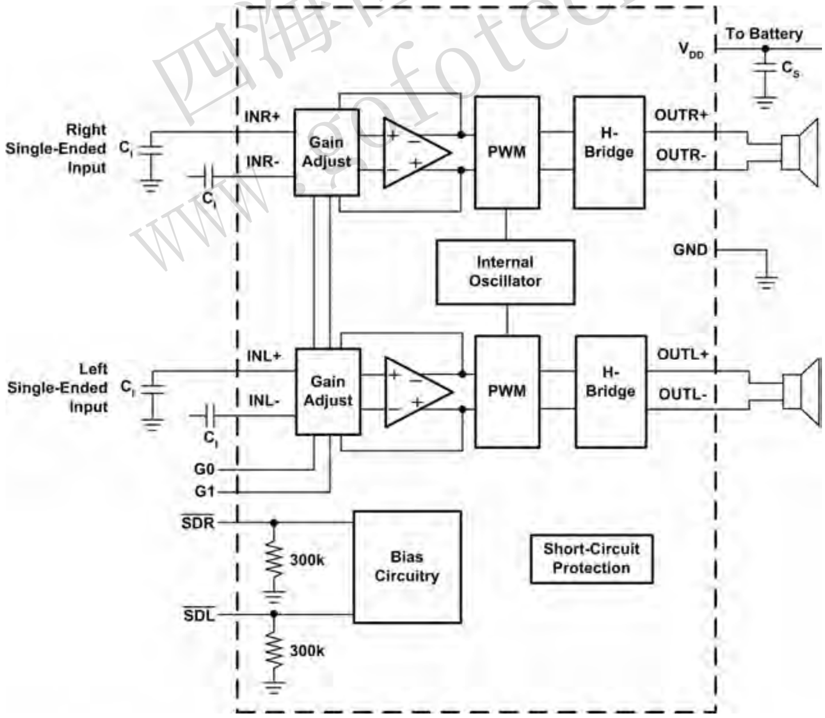
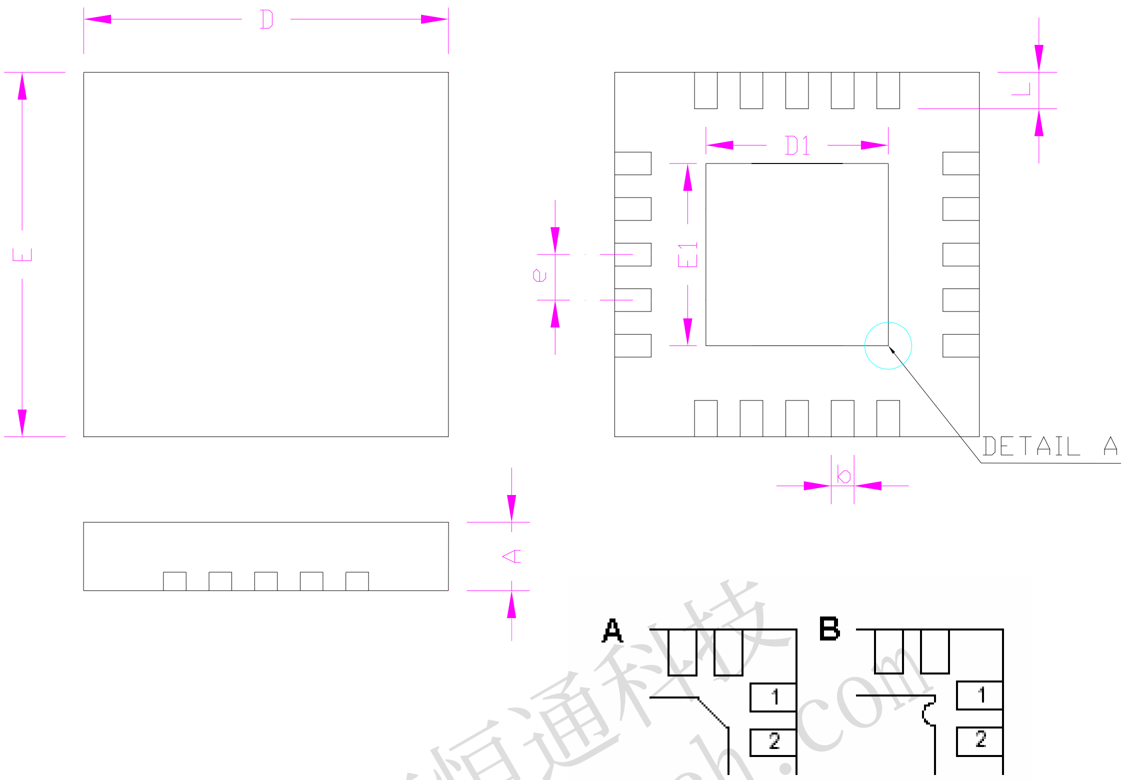


Figure33. Application Schematic With Single-Ended Input

Packaging Information

TQFN-20

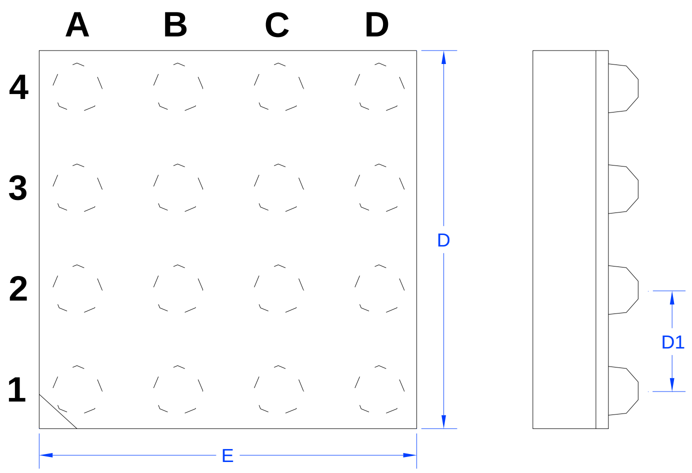


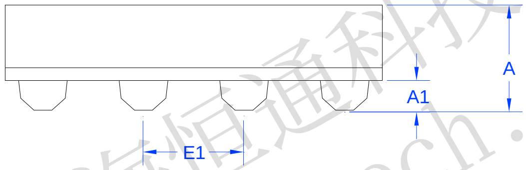
DETAIL A

Thermal Pad Option

SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
b	0.18	0.30	0.007	0.012
E	3.90	4.10	0.154	0.161
D	3.90	4.10	0.154	0.161
D1	2.70		0.106	
E1	2.70		0.106	
e	0.50		0.020	
L	0.30	0.50	0.012	0.020

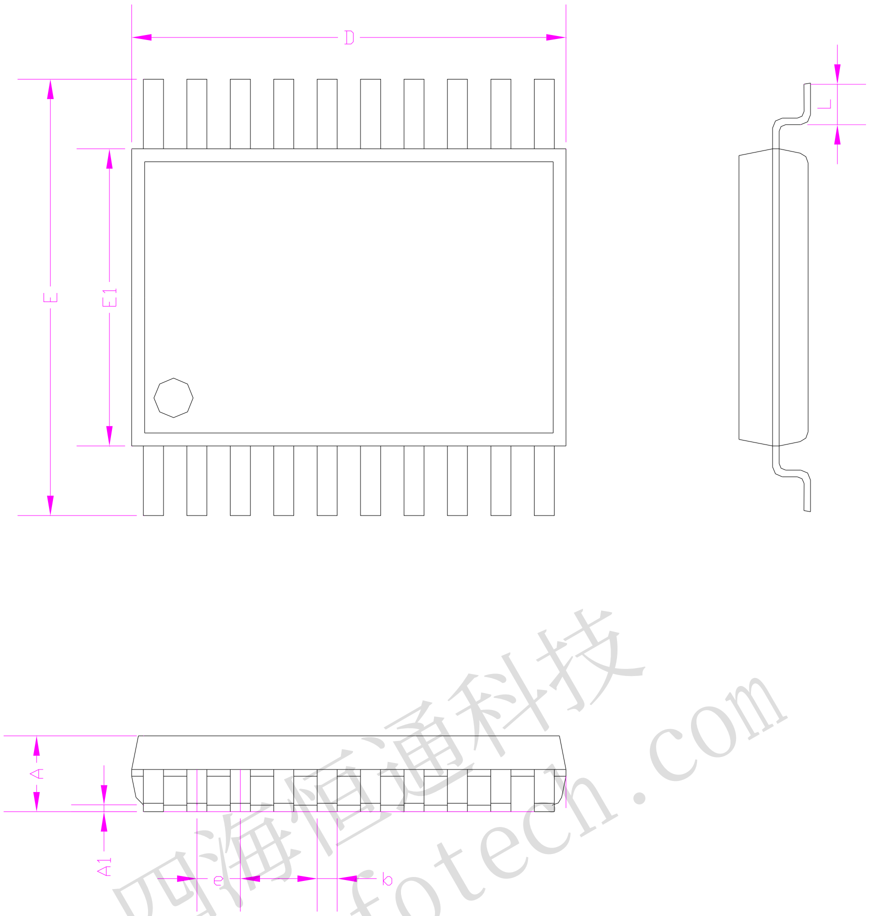
WCSP-16





SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	0.675	-	0.027
A1	0.15	0.35	0.006	0.014
D	2.01	2.11	0.079	0.083
D1	0.50		0.020	
E	2.01	2.11	0.079	0.083
E1	0.50		0.020	

TSSOP-20



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40		0.173	
D	6.50		0.256	
E	6.20	6.60	0.244	0.260
e	0.65		0.026	
L	0.45	0.75	0.018	0.030